What is Claimed is:

1. A nonvolatile FeRAM control device, comprising:

a pumping voltage controller configured to output a pumping voltage control signal by receiving a power voltage control signal having a different output level according as a power voltage region where a power voltage belongs, when the power control signal is applied;

a cell plate voltage controller configured to selectively output a cell plate pumping voltage control signal depending on states of the power voltage control signal, when a cell plate control signal is applied;

a write enable voltage controller configured to selectively output a write enable pumping voltage control signal depending on states of the power voltage control signal, when a write enable control signal is applied; and

a register array including a plurality of unit registers configured to boost and output voltage levels of data stored in a nonvolatile ferroelectric capacitor depending on voltage levels of the pumping voltage control signal, the cell plate pumping voltage control signal and the write enable pumping voltage control signal.

2. The nonvolatile FeRAM control device of claim 1,

wherein the pumping voltage controller outputs the pumping voltage control signal by pumping the power voltage as a pumping voltage level when the power voltage belongs to a low voltage region, and outputs the pumping voltage control signal as a power voltage level when the power voltage belongs to a high voltage region.

3. The nonvolatile FeRAM control device of claim 2, wherein the pumping voltage controller comprises:

a first logic device configured to logically operate the power voltage control signal and the power control signal;

a first delay unit configured to delay and logically reverse an output signal of the first logic device;

a first MOS capacitor configured to selectively pump a voltage level of the pumping voltage control signal depending on output states of the first delay unit;

a first driver configured to be connected between an output terminal of the first MOS capacitor and a ground terminal, and to selectively output a first driving signal in response to an output signal of the first logic device; and

a first driving device configured to be connected between an output terminal of the first MOS capacitor and a

power voltage, and to selectively precharge an output terminal of the first MOS capacitor depending on states of the first driving signal.

4. The nonvolatile FeRAM control device of claim 1, wherein the cell plate voltage controller comprises:

a second delay unit configured to output a first delay signal by delaying the cell plate control signal for a predetermined time;

a first pumping unit configured to output a first pumping signal having a pumping voltage level by pumping a power voltage in response to the first delay signal when the power voltage control signal is applied; and

a first level controller configured to output the cell plate pumping voltage control signal by level-shifting the first pumping signal and the cell plate control signal.

5. The nonvolatile FeRAM control device of claim 4, wherein when the cell plate control signal is inputted as a high level in the low voltage region, the cell plate voltage controller outputs the cell plate pumping voltage control signal as a power voltage level for a delay time of the second delay unit, and the cell plate voltage controller outputs the cell plate pumping voltage control

signal as a pumping voltage level after the delay time.

6. The nonvolatile FeRAM control device of claim 1, wherein the write enable voltage controller comprises:

a fourth delay unit configured to output a second delay signal by delaying the write enable control signal for a predetermined time;

a second pumping unit configured to output a second pumping signal having a pumping voltage level by pumping a power voltage in response to the second delay signal when the power voltage control signal is applied; and

a second level controller configured to output the write enable pumping voltage control signal by level-shifting the second pumping signal and the write enable control signal.

7. The nonvolatile FeRAM control device of claim 6, wherein when the write enable control signal is inputted as a high level in the low voltage region, the write enable voltage controller outputs the write enable pumping voltage control signal as a power voltage level for a delay time of the fourth delay unit, and the write enable voltage controller outputs the write enable pumping voltage control signal as a pumping voltage level after the delay time.

8. The nonvolatile FeRAM control device of claim 1, wherein each unit register comprises:

a first pumping voltage driver configured to be formed on a N-well region separated from other N-well regions of adjacent circuits, and to amplify and pull up both nodes of the unit register by receiving the pumping voltage control signal and a pull-up enable signal;

an equalizing unit configured to equalize both nodes of the unit register in response to an equalizing signal;

a first write enable pumping driver configured to output a voltage of a bitline into both nodes of the unit register in response to the write enable pumping voltage control signal;

a first ferroelectric capacitor unit configured to be connected between both nodes of the unit register and a cell plate, and to receive the cell plate pumping voltage control signal;

a first voltage driver configured to pull down both nodes of the unit register;

a first pull-down driving device configured to apply a ground voltage to the first voltage driver in response to the pull-down enable signal; and

a plurality of second ferroelectric capacitors

configured to be connected between both nodes of the unit register and a ground terminal, and to regulate capacitor load of the both nodes.

9. The nonvolatile FeRAM control device of claim 8, wherein the first pumping voltage driver comprises:

a pull-up driving device configured to selectively apply the pumping voltage control signal in response to the pull-up enable signal; and

a pair of PMOS transistors having a latch structure configured to have a source connected in common to the pull-up driving device and to have each gate cross-coupled with a drain,

wherein the pull-up driving device is connected to the pair of PMOS transistors in an individual N-well region.

10. The nonvolatile FeRAM control device of claim 1, wherein each unit register comprises:

a second pumping voltage driver configured to be formed on a N-well region separated from other N-well regions of adjacent circuits, and to amplify and pull up both nodes of the unit register by receiving the pumping voltage control signal and a pull-up enable signal;

a second write enable pumping driver configured to

output a voltage of a bitline into both nodes of the unit register in response to the write enable pumping voltage control signal;

a second ferroelectric capacitor unit configured to be connected between both nodes of the unit register and a cell plate, and to receive the cell plate pumping voltage control signal;

a second voltage driver configured to pull down both nodes of the unit register; and

a second pull-down driving device configured to apply a ground voltage to the second voltage driver in response to the pull-down enable signal.

11. The nonvolatile FeRAM control device of claim 1, wherein each unit register comprises:

a third pumping voltage driver configured to be formed on a N-well region separated from other N-well regions of adjacent circuits, and to amplify and pull up both nodes of the unit register by receiving the pumping voltage control signal and a pull-up enable signal;

a third write enable pumping driver configured to output a voltage of a bitline to both nodes of the unit register in response to the write enable pumping voltage control signal;

a third ferroelectric capacitor unit configured to be connected between both nodes of the unit register and a cell plate, and to receive the cell plate pumping voltage control signal; and

a third voltage driver configured to pull down both nodes of the unit register.

12. The nonvolatile FeRAM control device of claim 1, wherein each unit register comprises:

a fourth pumping voltage driver configured to be formed on a N-well region separated from other N-well regions of adjacent circuits, and to amplify and pull up both nodes of the unit register by receiving the pumping voltage control signal and a pull-up enable signal;

a fourth write enable pumping driver configured to output a voltage of a bitline to both nodes of the unit register in response to a write enable signal when the write enable pumping voltage control signal is enabled;

a fourth ferroelectric capacitor unit configured to be connected between both nodes of the unit register and a cell plate, and to receive the cell plate pumping voltage control signal; and

a fourth voltage driver configured to pull down both nodes of the unit register.

13. The nonvolatile FeRAM control device of claim 12, wherein the fourth write enable pumping driver comprises:

a sixth NMOS transistor and a seventh NMOS transistor configured to output the write enable signal, respectively, in response to the write enable pumping voltage control signal applied through a gate; and

a eighth NMOS transistor and a ninth NMOS transistor configured to output a voltage of a bitline into both nodes of the unit register in response to the write enable signal applied through the sixth NMOS transistor and the seventh NMOS transistor.

14. The nonvolatile FeRAM control device of claim 1, wherein in a power-up mode, each unit register re-writes first data in the nonvolatile ferroelectric capacitor when the cell plate pumping voltage control signal is at a pumping voltage level and the pumping voltage control signal is at a power voltage level, and re-writes second data in the nonvolatile ferroelectric capacitor when the cell plate pumping voltage control signal is at a ground voltage level and the pumping voltage control signal is at a pumping voltage level.

15. The nonvolatile FeRAM control device of claim 1, wherein in a write program mode, each unit register writes third data in the nonvolatile ferroelectric capacitor when the cell plate pumping voltage control signal and the write enable pumping voltage control signal are at a pumping voltage level and the pumping voltage control signal is at a power voltage level, and writes fourth data when the cell plate pumping voltage control signal and the write enable pumping voltage control signal are at a ground voltage level and the pumping voltage control signal is at a pumping voltage level.

16. A nonvolatile FeRAM control device, comprising a pumping voltage driver configured to amplify and pull up both nodes of a unit register including a nonvolatile ferroelectric capacitor in response to a pumping voltage control signal inputted at a timing different from a power voltage control signal in a low voltage region,

wherein the pumping voltage driver is configured to be formed on a N-well region separated from other N-well regions of adjacent circuits, and to receive the pumping voltage control signal.

17. The nonvolatile FeRAM control device of claim 16, wherein the pumping voltage driver comprises:

a pull-up driving device configured to selectively output the pumping voltage control signal in response to a pull-up enable signal;

a pair of PMOS transistors configured to have a source connected in common to the pull-up driving device and to have each gate cross-coupled with a drain,

wherein the pull-up driving device is connected to the pair of PMOS transistors in an individual N-well region.

18. A nonvolatile FeRAM control device, comprising a pumping voltage controller configured to output a pumping voltage control signal for boosting an output signal of a unit register including a nonvolatile ferroelectric capacitor by pumping a power voltage in response to a power control signal,

wherein the pumping voltage controller outputs the pumping voltage control signal as the pumping voltage level by pumping a power voltage in a low voltage region, and the pumping voltage controller outputs the pumping voltage control signal as the power voltage level in a high voltage region depending on states of a power voltage control signal for determining generation of a pumping voltage.

19. The nonvolatile FeRAM control device of claim 18, wherein the pumping voltage controller comprises:

a logic device configured to logically operate the power voltage control signal and the power control signal;

a delay unit configured to delay and logically reverse an output signal of the logic device;

a MOS capacitor configured to be connected to an output terminal of the delay unit;

a driver configured to be connected between an output terminal of the MOS capacitor and a ground terminal, and to have a common gate connected to the output signal of the logic device; and

a driving device configured to be connected between the MOS capacitor and a power voltage terminal, and to have a gate to receive an output signal of the driver.

20. A nonvolatile FeRAM control device, comprising a cell plate voltage controller configured to output a pumping voltage control signal into a cell plate of a nonvolatile ferroelectric capacitor in a unit register depending on states of a power voltage control signal when a cell plate control signal,

wherein when the cell plate control signal is

inputted as a high level in a low voltage region where the power voltage control signal is at a high level, the cell plate voltage controller outputs the cell plate pumping voltage control signal as a power voltage level for a predetermined delay time, and outputs the cell plate pumping voltage control signal as a pumping voltage level after the delay time.

21. The nonvolatile FeRAM control device of claim 20, wherein the cell plate voltage controller comprises:

a delay unit configured to output a delay signal by delaying the cell plate control signal for a predetermined time;

a pumping unit configured to output a pumping signal having a pumping voltage level by pumping a power voltage in response to the delay signal when the power voltage control signal is applied; and

a level controller configured to control a voltage level of the cell plate pumping voltage control signal by level-shifting the pumping signal and the cell plate control signal.

22. A nonvolatile FeRAM control device, comprising a write enable voltage controller configured to output a

write enable pumping voltage control signal into both nodes of a unit register including a nonvolatile ferroelectric capacitor depending on states of the power votlage control signal when a write enable control signal is applied,

wherein when the write enable control signal is inputted as a high level in a low voltage region where the power voltage control signal is at a high level, the write enable voltage controller outputs the write enable pumping voltage control signal as a power voltage level for a predetermined delay time, and outputs the write enable pumping voltage control signal as a pumping voltage elevel after the delay time.

23. The nonvolatile FeRAM control device of claim 22, wherein the write enable voltage controller comprises:

a delay unit configured to output a delay signal by delaying the write enable control signal for a predetermined time;

a pumping unit configured to output a pumping signal having a pumping voltage level by pumping a power voltage in response to the delay signal when the power voltage control signal is applied; and

a level controller configured to control a voltage level of the write enable pumping voltage control signal by

level-shifting the pumping signal and the write enable control signal.

24. A nonvolatile FeRAM control device, comprising:

an I/O setup controller configured to set up activation or inactivation of a plurality of sub data I/O pins included in a plurality of data I/O pins;

a register array configured to comprise a plurality of unit registers including a nonvolatile ferroelectric capacitor, and to be selectively activated depending on the control of the I/O setup controller;

a data I/O controller configured to output a control signal for setting up an I/O pin by analyzing data applied from the register array; and

an I/O buffer configured to selectively activate the plurality of sub data I/O pins in response to a control signal applied from the data I/O controller.

25. The nonvolatile FeRAM control device of claim 24, wherein the register array further comprises:

a pumping voltage controller configured to output a pumping voltage control signal by receiving a power voltage control signal having a different output level according to a power voltage region where a power voltage belongs when a

power control signal is applied;

a cell plate voltage controller configured to output a cell plate pumping voltage control signal depending on states of the power voltage control signal when a cell plate control signal is applied; and

a write enable voltage controller configured to output a write enable pumping voltage control signal depending on states of the power voltage control signal when a write enable control signal is applied,

wherein voltages of data stored in the nonvolatile ferroelectric capacitor are boosted and outputted depending on voltage levels of the pumping voltage control signal, the cell plate pumping voltage control signal and the write enable pumping voltage control signal.

26. A nonvolatile FeRAM control device, comprising:

a sector protection setup controller configured to set up a sector protection region for protecting data written in a memory array region including a plurality of sector regions;

a register array configured to comprise a plurality of unit registers including a nonvolatile ferroelectric capacitor, and to be selectively activated depending on the control of the sector protection setup controller; and

a memory sector controller configured to control a corresponding sector of the memory array region by analyzing sector protection information applied from the register array.

27. The nonvolatile FeRAM control device of claim 26, wherein the register array comprises:

a pumping voltage controller configured to output a pumping voltage control signal by receiving a power voltage control signal having a different output level according to a power voltage region where a power voltage belongs when a power control signal is applied;

a cell plate voltage controller configured to output a cell plate pumping voltage control signal depending on states of the power voltage control signal when a cell plate control signal is applied; and

a write enable voltage controller configured to output a write enable pumping voltage control signal depending on states of the power voltage control signal when a write enable control signal is applied,

wherein voltages of data stored in the nonvolatile ferroelectric capacitor are boosted and outputted depending on voltage levels of the pumping voltage control signal, the cell plate pumping voltage control signal and the write

enable pumping voltage control signal.